Dr. J. KOKILA

No: 80 Shoba Enclave ,
RVS Nagar, RS puram second main road,
Khajamalai Road,
Tiruchirappalli -620023,
Tamil Nadu, INDIA
jk.cse09@gmail.com, kokilaj@iiitt.ac.in
https://sites.google.com/site/kokilajrsnitt/
https://scholar.google.com/citations?user=gn4elnUAAAAJ&hl=en
www.linkedin.com/in/dr-kokila-jagadeesh-29737684

EDUCATION

2014 – 2019 **Doctor of Philosophy under Visvesvaraya PhD Scheme with CUG 9.5**
Department of Computer Science and Engineering,
National Institute of Technology, Tiruchirappalli, Tamil Nadu, INDIA.
Thesis Title: *Enhancing Security and Reliability of Heterogeneous IPs for SoC FPGAs*
Supervisor: *Professor N. Ramasubramanian*

2008 – 2010 **Master of Engineering with CUG 8.7**
Department of Computer Science and Engineering,
Anna University Tiruchirappalli, Tamil Nadu, INDIA.
Thesis Title: *BSMRNN for speech processing using Haar wavelets*

2001– 2005 **Bachelor of Engineering with 77%**
Department of Computer Science and Engineering,
Anna University Chennai, Tamil Nadu, INDIA.
Project Title: *System and Mobile Networking using Infrared*

HONOURS & AWARDS

2005, 2010 **First class and Distinction** in B.E. and M.E. CSE.

2005 **College First in B.E. CSE**

2010 **Rank holder in M.E. CSE**

2014 **First Visvesvaraya PhD Scheme in Department of CSE at NITT**

2018 Student coordinator award for FDP in NITT

2019 **Certificate of Recognition award** for publishing paper in IEEE Transactions on Very Large Scale Integration Systems.

TEACHING EXPERIENCE

2023– · · · · **Indian Institute of Information Technology, Tiruchirappalli** as Assistant Professor, in Department of Computer Science and Engineering.

2021 – 2023 **Indian Institute of Information Technology, Allahabad** as Assistant Professor Grade -II, Level-10 in Department of Information Technology at Network security and Cryptography Lab.

2013 – 2014 **National Institute of Technology, Tiruchirappalli** as Temporary Faculty, in Department of Computer Science and Engineering.

2012 – 2013 **K.RamaKrishnan College of Technology,Trichy affiliated to Anna University, Chennai** as Assistant Professor, in Department of Computer Science and Engineering.

TEACHING EXPERIENCE (continued)

2010 – 2012 **Oxford Engineering College, Trichy affiliated to Anna University, Chennai** as Senior Lecturer, in Department of Computer Science and Engineering.

2006 – 2008 **Saranathan college of Engineering affiliated to Anna University, Chennai** as Lecturer, in Department of Computer Science and Engineering.

2005– 2006 **M. Kumarasamy college of Engineering ,Karur affiliated to Anna University, Chennai** as Lecturer, in Department of Computer Science and Engineering.

RESEARCH & TEACHING INTEREST

RESEARCH INTEREST

- **Hardware Security**
- **Blockchain Technology**
- **SoC Platform and FPGA**
- **IoT Security at edge-level**
- **Computer Architecture**

TEACHING INTEREST

- **Blockchain and Cryptocurrency**
- **Information Security**
- **Cybersecurity and Digital Forensics**
- **Embedded Security**
- **Theory of computing**
- **Computer Architecture**
- **Data Structures and algorithm**
- **Compiler Design**
- **Operating System**

ACADEMIC & ADMINISTRATIVE EXPERIENCE

2005- 2008 **Private College** Mentor for 5 set of undergraduates

2010 -2014 **Guided projects for undergraduates and Post graduates**

2005 - 2014 **In-charge for Time table and course work**

2021 **Member of Department Post-Graduate Committee of IT at IIIT, Allahabad**

Guided Min-Project for 6 group of Students in Department of Information Technology, at IIIT, Allahabad

2022 Guided Project for 3 group of Students B.Tech and 4 individual Project for M. Tech. in Department of Information Technology, at IIIT, Allahabad

Invited Talks & Events Organized

Invited Talks

- **Cybersecurity threat** in the FDP on Cyber Physical security for Critical Infrastructure sponsored by AICTE Training and ATAL at IIIT, Allahabad, Aug 4, 2021
- **Security threats and Attacks** in the cyber security webinar series 2 at Indian institute of Information Technology, Kottayam, Nov 20 , 2021
- **IoT Security** in the Workshop on Cyber Security: Basics and Emerging Trends at IIIT, Allahabad, Dec 15, 2021

Invited Talks & Events Organized (continued)

- **Security Issues in IoT Edge Computing** in one-week online AICTE-ISTE Faculty Refresher on Embedded Systems, IoT, Pervasive Computing at Talla Padmavathi College of Engineering Kazipet, Warangal, Dec 8, 2021
- **Machine Learning approaches to secure IoT Edge Computing** in the Two Week FDP on AI & Machine Learning for IOT and Computer Vision Applications through E & ICT NIT Warangal at Anurag University, Hyderabad, Jan 20, 2022.
- **Security solutions for IoT edge Computing** in the 3 Days online Faculty development program on "Collective Technologies on AI and IoT with security" at CARE College of Engineering, Trichy, March 03, 2022

Events Organized

- As Organizing Committee Member in the 9th International Conference on Big Data Analytics (BDA 2021)
- As coordinator in Workshop on Advancement in Blockchain Technology – 04 march, 2022

RESEARCH PUBLICATIONS

Journal Articles

1. Rajaram, S., Vollala, S., Ramasubramanian, N., & Kokila, J. (2021). *Enhanced and Secured Random Number Generation for eUASBP. International Journal of System Assurance Engineering and Management*.
2. Jagadeesh, K., & Natarajan, R. (2019). Lightweight signature scheme to protect intellectual properties of internet of things applications in system on chip field-programmable gate arrays. *Turkish Journal of Electrical Engineering & Computer Sciences*, *27*, 3500–3515. doi:10.3906/elk-1811-97
3. Kokila, J., & Ramasubramanian, N. (2019). *Enhanced Authentication Using Hybrid PUF with FSM for Protecting IPs of SoC FPGAs. Journal of Electronic Testing*, *35*, 543–558. doi:10.1007/s10836-019-05808-w
4. Kokila, J., Ramasubramanian, N., & Naganathan, N. (2019). *Resource Efficient Metering scheme for protecting SoC FPGA device and IPs in IOT applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *27*, 2284–2295. doi:10.1109/TVLSI.2019.2926788
5. Kokila, J., Das, A. M., Begum, B. S., & Ramasubramanian, N. (2019). *Hardware Signature Generation Using a Hybrid PUF and FSM Model for an SoC Architecture. Periodica Polytechnica Electrical Engineering and Computer Science*, *63*, 244–253. doi:https://doi.org/10.3311/PPee.13424
6. Kokila, J., Ramasubramanian, N., & Thamma, R. (2018). *Dynamic Estimation of Temporary Failure in SoC FPGAs for heterogeneous applications. J. Universal Comput. Sci*, *24*, 1776–1799. doi:10.3217/jucs-024-12-1776

Conference Proceedings

1. Aravindan, M. et al. (2022). Practical challenges in simulating strong pufs. In *2022 ieee ias global conference on emerging technologies (globconet)* (pp. 471–476). IEEE.
2. Roy, A., Kokila, J., Ramasubramanian, N., & Begum, S. B. (2022). Random number generation for pki using controlled anderson puf. In *2022 ieee international conference on public key infrastructure and its applications (pkia)* (pp. 1–6). IEEE.
3. Roy, A., Panwar, P., Kokila, J., Ramasubramanian, N., & Begum, B. S. (2022). Detection of hardware trojan using cnn with residual network. In *2022 ieee 6th conference on information and communication technology (cict)* (pp. 1–6). IEEE.

4. Kokila, J., Chithra, S., & Ramasubramanian, N. (2021). Side-channel analysis using deep learning on hardware trojans. In *Iop conference series: Materials science and engineering* (Vol. 1049, p. 012018). IOP Publishing.

5. Chithra, C., Kokila, J., & Ramasubramanian, N. (2020). Detection of hardware trojans using machine learning in soc fpgas. In *2020 IEEE International Conference on Electronics, Computing and Communication Technologies* (*CONECCT*) (pp. 1–7). IEEE.

6. Kokila, J., Chellam, M. B., Das, A. M., & Ramasubramanian, N. (2017). Light weight two-factor authentication using hybrid puf and fsm for soc fpga. In *International conference on next generation computing technologies* (pp. 381–395). Springer.

7. Manjith, B., Kokila, J., & Natarajan, R. (2017). Adaptive dynamic partial reconfigurable security system. In *International conference on next generation computing technologies* (pp. 430–439). Springer.

8. Kokila, J., Ramasubramanian, N., & Indrajeet, S. (2016). A survey of hardware and software co-design issues for system on chip design. In *Advanced computing and communication technologies* (pp. 41–49). Springer.

Books and Chapters

1. Ramasubramanian, N., & Kokila, J. (2021). *Security of internet of things nodes: Challenges, attacks, and countermeasures: Study of hardware attacks on smart system design lab*. CRC Press.

RESEARCH PROPOSALS SUBMITTED

UGC - New Recuritment

- Proposal Title: PUF based Key Management to Mitigate Cryptographic Trojans on Multicore SoC,
  Submitted: Oct 2022.
  Responsible: Principle Investigator

SERB CORE

- Proposal Title: Dynamic Reconfigurable Key Orchestration of Adaptable Heterogeneous crypto Accelerators in CPU centric Ecosystem
  Submitted: March 2023.
  Responsible: Principle Investigator

SEMINAR, TRAINING AND WORKSHOPS ATTENTED

2014
- **Two weeks ISTE Workshop on Computer Programming** conduct by IIT, Bombay, under the National Mission on Education through ICT (MHRD, Govt. of India) during $16^{th} - 21^{st}$ June.

2015
- **Think Parallel: Parallel Programming for Engineers & Scientists** is a 5-days training programme conducted by CDAC, Bangalore during $20^{th} - 24^{th}$ July.
- **Advanced Embedded System Design on Zynq using Vivado targeting Zed Board** is a workshop conducted by NIT, Trichy during $27^{th} - 28^{th}$ August.

2016
- **System Design on Zynq using SDSoC** is a workshop conducted by IIT Madras during $1^{st} - 3^{rd}$ January
- **Visvesvaraya PhD Scheme Paper Presentation and Review Meeting** conducted by Indian Institute of Technology Bombay (IITB),in collaboration with DEITY during 13^{th}&14^{th} Oct.

2018
- **Xilinx Soc:FPGA Based Design** is a Faculty Development programme conducted by IIT Guwahati in collaboration with NIT, Tiruchirapalli during $30^{th} July - 3^{rd}$ August.

2020
- **Online Short Course on Deep Learning** organized by IEEE Computer Society Chapter and IEEE Student Branch of NITT in association with Pantech Solutions during $6^{th} - 10^{th}$ July.

SEMINAR, TRAINING AND WORKSHOPS ATTENTED (continued)

- **Online Short Course on "VLSI Physical Design using Cadence Innovus Tool"** organized by he Department of Electronics and Communication Engg, of St. Joseph'st College of Engg, Chennai during $20^{th} - 24^{th}$ July, 2020

MEMBERSHIP

- **IEEE Member**
- **IEEE Young Professional**
- **IEEE Women in Engineering**

REFERENCES

Prof.N. Ramasubramanian
Department of Computer Science and Engineering,
National Institute of Technology,
Trichy, INDIA.
Mobile No.: +91-431-250 3204
nrs@nitt.edu

Prof.O.P.Vyas
Professor(Information Technology), and
Coordinator(Business Informatics),
Indian Institute of Information Technology,
Allahabad (UP),INDIA
Mobile No.: 9839321091
opvyas@iiita.ac.in

Prof.Ravindra Thamma
Chair of Manufacturing and Construction Management Department,
School of Engineering, Science and Technology,
Central Connecticut State University,
1615 Stanley Street,
New Britain, CT 06053
Mobile No.: (860) 832 3516
thammarav@ccsu.edu